Ministério da
Ciência e Tecnologia

INPE-16569-TAE/78

HIGH STEP-UP AND HIGH EFFICIENCY POWER PROCESSOR

Renato Oliveira de Magalhães

Relatório apresentado após conclusão do estágio realizado no Laboratório de Eletrônica de Potência da Universidade de Padova - Itália

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Abstract

This work is the analysis, simulation and experimental validation of a high step-up and high efficiency dc-dc converter.

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Chapter 1

Introduction

The processing of power has become in recent years more challengeable as new requirements for higher efficiency are now one of the main priorities in system development. Currently, the use of switching power supply represents the majority of solutions in many applications but the designer is always facing the problem of finding the most feasible solution for its necessity. This report will present the analysis, simulation and prototype validation of a high step up and high efficiency power supply topology and discuss about its advantages and drawbacks.

1.1 Context and motivation

Batteries and photovoltaics panels are usually required to step up their voltages in some applications where no galvanic isolation is required. Some of the examples[FCL] are the ac utility grid generated by solar energy and the use of batteries to provide lighting, by means of High Intensity Discharge (HID) lamps, as shown in Fig. 1.1. In these kind of applications a high step up voltage ratio is required which results in two major concerns. The first is the large input current that this kind of topology needs to handle. Therefore, low voltage rated devices with low R_{DS} are necessary to reduce conduction losses. The second concern is the high output voltage which implies severe reverse recovery in output rectifier diode.

Conventional solutions such as boost topology fail to achieve the requirements of high voltage gain and high efficiency since both requirements degrade with the increase of the duty cycle necessary to step the input voltage to a much higher output.

1.2 Contents

The main body of this report is divided as follows.

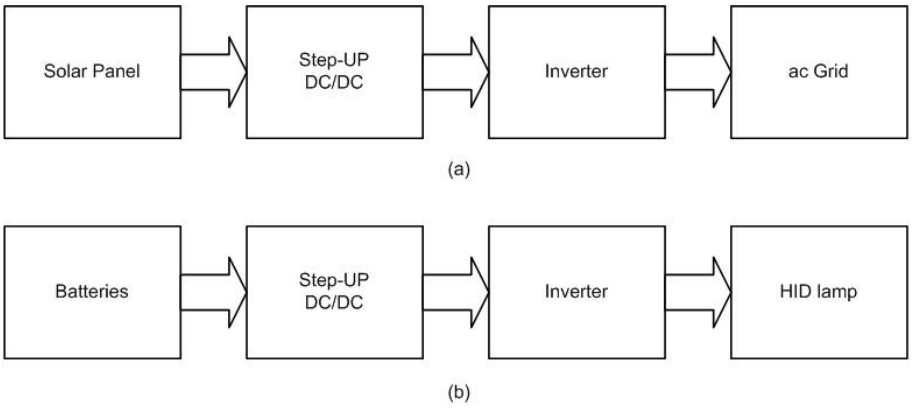

Figure 1.1: Applications of Step-Up Converters: (a) Grid-connected photovoltaic panels (b) HID lamp ballast

Chap. 2 explains the theoretical functioning of the topology. Chap. 3 presents some results of simulation based on SPICE and also using the toolbox PLECS in Simulink/Matlab. Chap. 4 shows waveforms and measurements done in the prototype manufactured. The Conclusion, in Chap. 5, summarises what's been achieved, the open questions and what could be done next.

At the end of this report there is a list of all bibliography used in this work.

Chapter 2

Topology Analysis

In this chapter the fundamental topology used to achieve high step up voltage ratio and high efficiency will be presented. An approximated theoretical analysis of the losses presented in this kind of converter is derived. With that knowledge in hand, some small modifications that can be done in the original topology, in order to improve efficiency and voltage stress on the output diode will be discussed.

2.1 Description

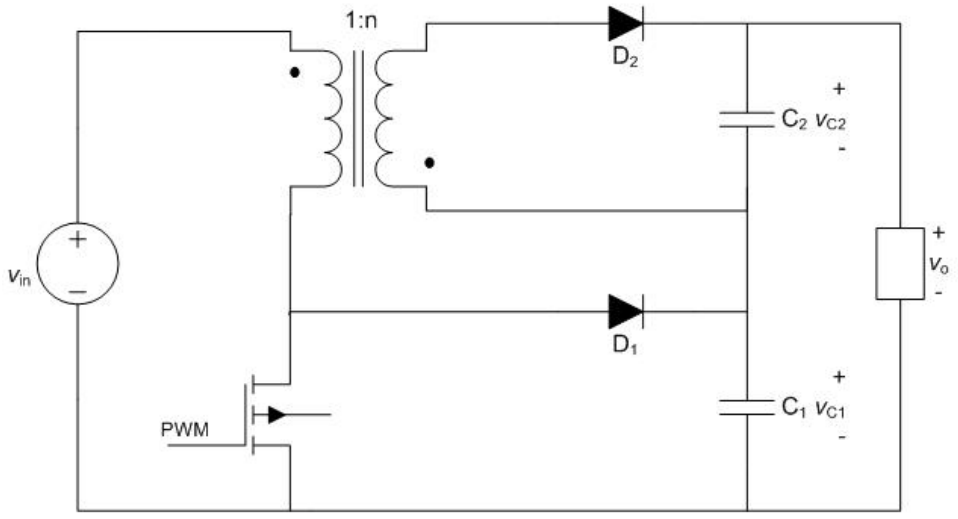

Figure 2.1: Flyback-Boost Topology.

The basic structure of the topology to be studied is shown in Fig. 2.1.

It‘s a flyback with a clamp in parallel with the mosfet. Since this clamp, together with the mosfet and transformer, is topological equivalent to a boost, we will be referring to this topolgy as Flyback-Boost, for the sake of convenience. In this configuration, the capacitor used to clamp the energy stored in the primary leakage inductance of the transformer is connected in series with the flyback output capacitor. This improves efficiency since we are not losing the energy of leakage inductance as well as contribute to increase the output voltage, leading to a high input to output voltage ratio. With this scheme we lose the galvanic isolation between input and output, which can be acceptable to some applications such as the first stages of dc-ac inverters, just to name a few.

2.2 Converter Operation

The condition to be analysed is the flyback section working in continuous conduction mode and the boost section working in discontinuous conduction mode. We should refer to Fig. 2.2 and Fig. 2.3 as they represent, respectively, the modes of operation and associated waveforms. The transfomer of Fig. 2.1 is replaced by its equivalent electrical model. Taking into account the parasitic primary leakage inductance, there are four distinct states or modes as shown. Prior to the instant t_0 the topology is in mode 4 with diode D_2 conducting and the energy stored in the magnetizing inductance being transferred to capacitor C_2. At instant t_0 the switch is closed and then follows the sequence of modes as it will be described next.

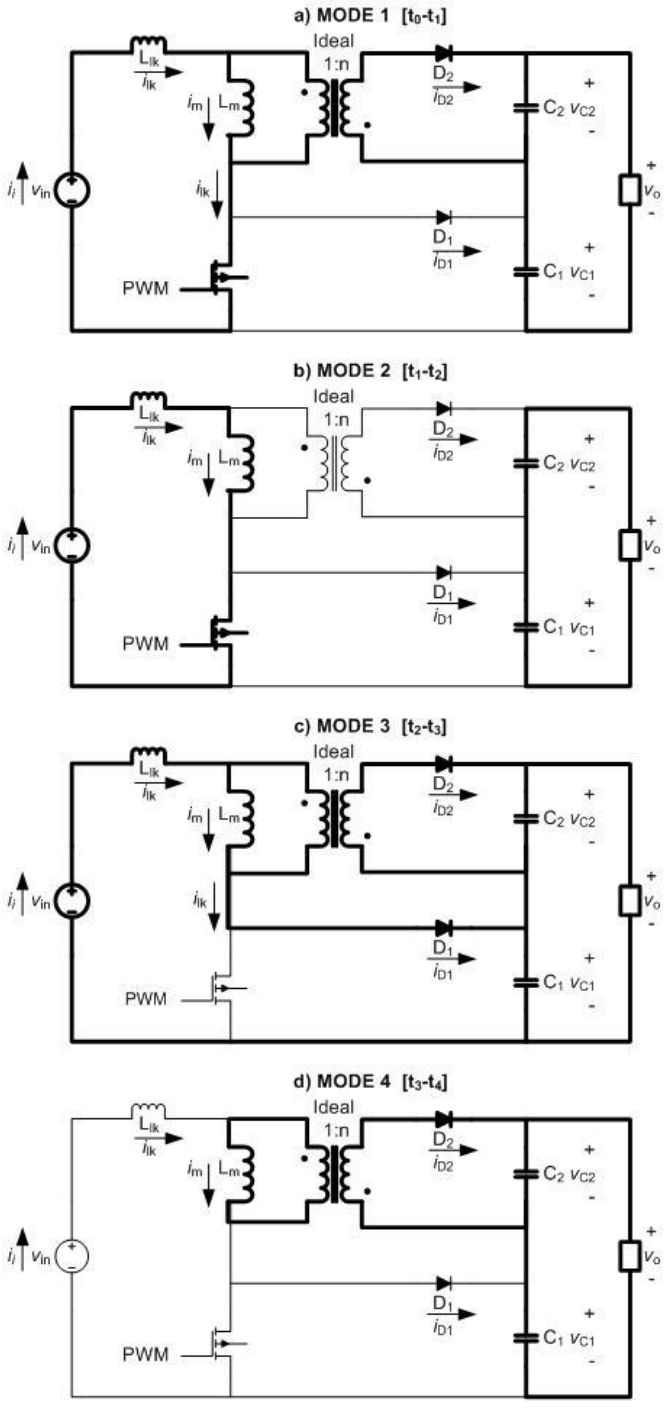

Figure 2.2: Flyback-Boost Modes.

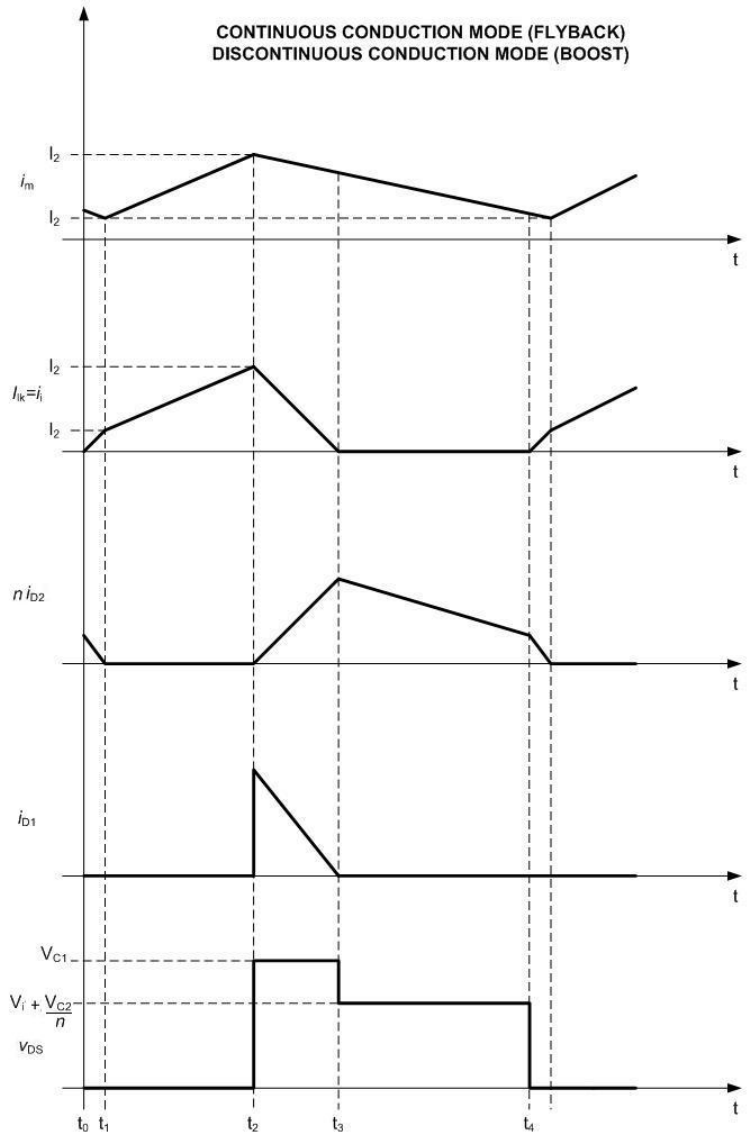

Figure 2.3: Flyback-Boost Waveforms.

MODE 1 [t_0-t_1]:

When the switch is closed, diode D_2 does not cut off instantaneously due to the presence of primary leakage inductance. Since this diode is still conducting, the voltage on capacitor C_2 is reflected back in the primary side, with transformer voltage ratio n and its polarity inverted. The input current, which is equal to the leakage inductance current, starts to increase with positive slope determined by

$$\frac{\Delta i_{lk}}{\Delta t} = \frac{v_{in} + v_{C_2}/n}{L_{lk}} \tag{2.1}$$

Magnetizing current continues do decrease with negative slope determined by

$$\frac{\Delta i_m}{\Delta t} = -\frac{v_{C_2}/n}{L_m} \tag{2.2}$$

Only when the leakage inductance current reaches the value of magnetizing current, diode D2 cuts off and starts mode 2.

MODE 2 [t_1-t_2]:
Now, D_2 is off, the load is supplied by capacitors C_1 and C_2 only. The leakage inductance current equals the magnetizing inductance current and they increase with positive slope slope determidend by

$$\frac{\Delta i}{\Delta t} = \frac{v_{in}}{L_m + L_{lk}} \tag{2.3}$$

MODE 3 [t_2-t_3]:
At instant t_2 the switch is opened, causing diodes D_1 and D_2 to conduct. During this interval, the energy stored in the leakage inductance is discharged into capacitor C_1. The leakage inductance current starts do decrease with negative slope given by

$$\frac{\Delta i_{lk}}{\Delta t} = -\frac{v_{C_1} - v_{C_2}/n - v_{in}}{L_{lk}} \tag{2.4}$$

The magnetizing current starts to decrease according to 2.2. As the leakage inductance current decreases, the diode D_2 current, reflected in the primary side of the ideal transformer, starts to increase. It reaches the magnetizing current once the leakage inductance current goes to zero. At this instant, diode D_1 is turned off.

MODE 4 [t_3-t_4]:
Once diode D_1 is turned off, the magnetizing current continues to decrease, transfering energy to the secondary side, until the switch is turned on again at instant t_4 and the process starts over again.

At this point would be interesting to have some simulation data. Refer to chapter 3 section 3.1 for some results of what have been explained so far.

2.3 Power Losses Analysis

The objective of this section is to understand the power losses mechanisms of this topology and how to mitigate their effects. Generally, losses are largely found in switching components, such as mosfets and diodes, and in a lesser extent in inductors and capacitors. Also important to notice is the effect of duty cycle since the longer any switching power supply remains in a particular interval, the greater the relative losses are that coincides with that interval.

We will divide this section in different categories and discuss only the main contributors of losses in this topology. They are listed in the next subsections.

2.3.1 Conduction Losses

MOSFET

The R_{DS} has a fundamental role in conduction loss. Obviously, the losses increases with power (current) as well as with the time each component remains in the ON state (effect of the duty cycle). R_{DS} increases with drain-source breakdown voltage and therefore, it's important not oversize a mosfet, as this can introduce efficiency penalties compared to a smaller properly chosen device. The mosfet conduction loss can be estimated using the equation bellow:

$$P_{C_{mosfet}} = R_{DS} \times i^2_{DS_{rms}} \tag{2.5}$$

DIODES

In the case of a diode, the forward voltage V_F has a fundamental role in conduction loss. Also obviously is the fact that the losses increases with current and the time the component remais in the ON state (effect of the duty cycle). Regarding switching diodes, they are usually named FAST (t_{rr} $\approx$ 100ns), SUPER FAST, ULTRAFAST recovery ($t_{rr} \approx$ 10ns). They tend to have large voltage drops but are available with large voltage and current ratings which are suitable for the kind of application we are dealing with.

Altough schottky diodes offer virtually non existent recovery times and low V_F (0.4V to 1V) they are not available with high voltage ratings.

The diode conduction losses can be estimated using the equation bellow:

$$P_{C_{diode}} = V_F \times i_{D_{avg}} \tag{2.6}$$

2.3.2 Switching Losses

MOSFET

In the following discussion we define the parasitic capacitance between drain and source of the mosfet as C_{drain}, which is the sum of C_{oss} and C_{xt}, respectively meaning mosfet output capacitance and transformer winding capacitance. The mosfet turns on with zero current. Nevertheless, there is a non zero voltage due to C_{drain}. The energy stored by this capacitance at the end of previous cycles is dissipated in the mosfet at the beggining of the turn on interval. This dissipated energy is proportional to the square of the voltage on this parasitic capacitance. At turn off there is a non zero current situation and the evaluation of switching loss at this instant can be aproximated by the waveform behaviuor shown in Fig. 2.4

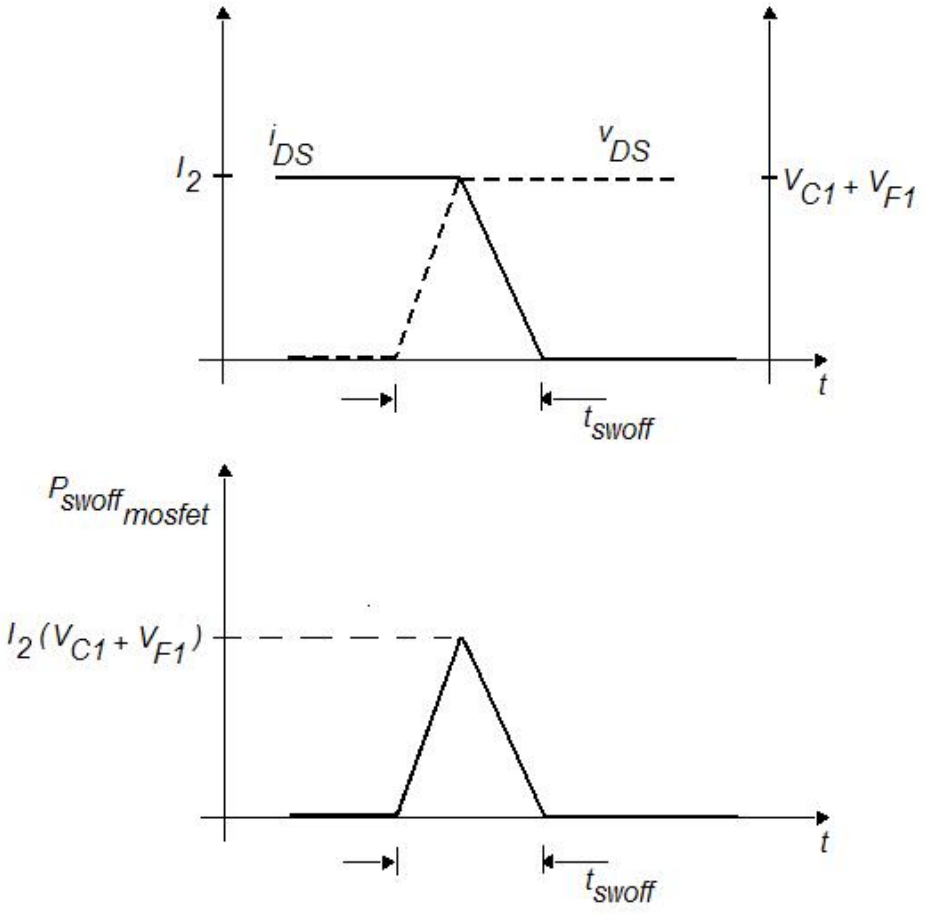

Figure 2.4: Instantaneous Mosfet Switching Loss at Turn-Off.

The mean value of this power loss over a switching cycle is given by

equation 2.7

$$< P_{swoff_{mosfet}} >= \frac{1}{T}\int_0^T P_{swoff_{mosfet}} dt = \frac{1}{T} t_{swoff} \times I_2 \times (V_{C1} + V_{F1}) \times 0.5 \tag{2.7}$$

Therefore, the approximated switching losses at turn off can be given by equation 2.8.

$$< P_{swoff_{mosfet}} >= 0.5 \times I_2 \times (V_{C1} + V_{F1}) \times t_{swoff} \times f_s \tag{2.8}$$

2.3.3 Power Losses Calculations

We can now use the results of simulation presented in chapter 3 and shown in Fig. 3.3 to calculated the losses discussed in the previous sections. This will give only an aproximated idea of the main contributor to losses in this topology. With the toolbox PLECS it's easy to obtain some points of interest such as rms currents, i_{ds} current prior to turn-off (and named I_2 in Fig. 2.4) and capacitor C_1 voltage. The time for the mosfet switch off can be estimated from Fig. 4.3 in chapter 4. These values, other components parameters and the resulted calculation are in table 2.1.

Table 2.1: Simulation Results

i_{lk} rms	i_{D2} rms	i_{D1} rms	i_{ds} rms	I_2	v_{C1}	t_{swoff}
8.2A	0.4A	0.4A	8.0A	13.6A	70.6V	50ns
P_{in} rms	R_{ds}	V_F	$P_{C_{mosfet}}$	$P_{C_{D1}}$	$P_{C_{D2}}$	$P_{sw_{mosfet}}$
164W	50mΩ	0.8V	3.2W	0.32W	0.32W	2.4W

2.4 Modified Topology

It has been observed that at the mosfet turn-on, a large amount of voltage ringing take place at the flyback diode in the secondary side. Although effective snubbers can be designed, this is not the desired situation since it represents more losses of energy. To overcome this ringing without the use of a snubber, the diode D_3 was introduced[GSN] in the topology, as shown in Fig. 2.5 and it will be referred to from now on as the clamping diode.

The idea behind the clamping diode is as follow. Let us call the voltage of the tranformer primary side reflected on the secondary as v_s. Then the voltage on diode D_3, from its cathode to anode, is named V_{D3} and is equal to

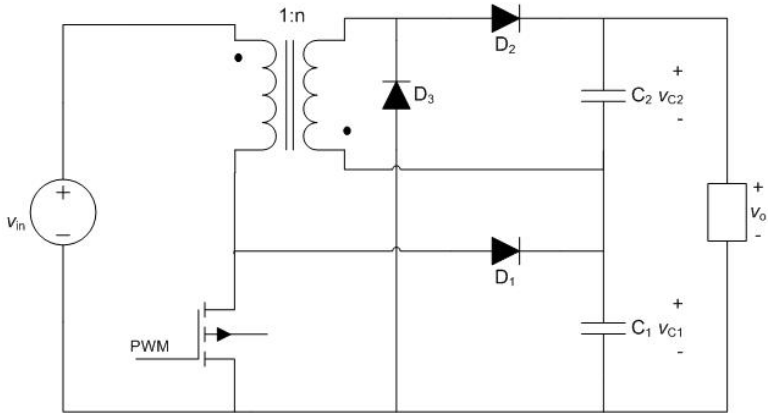

Figure 2.5: Modified Topology With Clamping Diode.

$$v_{D3} = v_s - v_{C1} \tag{2.9}$$

Suppose now that the voltage v_s is higher than the voltage across capacitor C_1. Then diode D_3 is forward biased and connects capacitor $C1$ directly across the secondary side of the transformer as shown by the bold electrical path in Fig. 2.6 and therefore clamping the voltage at this location.

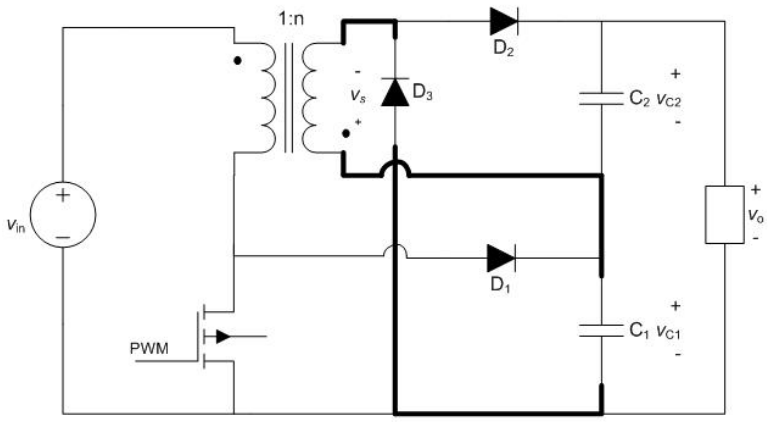

Figure 2.6: Functioning of the Clamping Diode.

Referring to Fig. 2.7 , the equations that governs this new topology in all its different states of operation were derived by[GSN] and can be divided as stated next.

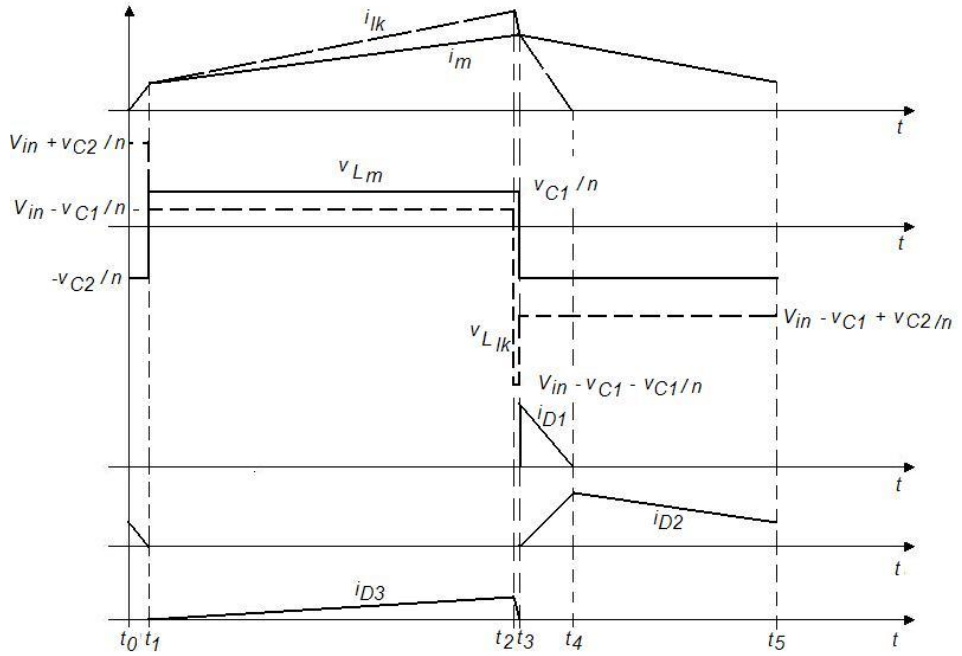

Figure 2.7: Waveforms of the Modified Topology.

MODE 1 [t_0-t_1]:

When the switch is closed, diode D_2 does not cut off instantaneously due to the presence of primary leakage inductance. Since this diode is still conducting, the voltage on capacitor C_2 is reflected back in the primary side, with transformer voltage ratio n and its polarity inverted. The input current, which is equal to the leakage inductance current, starts to increase with positive slope determined by eq. 2.10

$$\frac{\Delta i_{lk}}{\Delta t} = \frac{v_{in} + \frac{v_{C_2}}{n}}{L_{lk}} \tag{2.10}$$

Magnetizing current continues to decrease with negative slope determined by eq. 2.11

$$\frac{\Delta i_m}{\Delta t} = -\frac{\frac{v_{C_2}}{n}}{L_m} \tag{2.11}$$

Only when the leakage inductance current reaches the value of magnetizing current, diode D2 cuts off and starts mode 2. The equivalent circuit is shown in Fig. 2.8(A)

MODE 2 [t_1-t_2]:

Now, D_2 is off and we assume that the voltage at the secondary side of the transformer is higher than v_{C1}. Therefore diode D_3 turns on and energy is transferred directly to capacitor C_1. The leakage inductance current slope is determided by eq. 2.12.

$$\frac{\Delta i_{lk}}{\Delta t} = \frac{v_{in} - \frac{v_{C_1}}{n}}{L_{lk}} \tag{2.12}$$

The magnetizing inductance current slope is determined by eq 2.13.

$$\frac{\Delta i_m}{\Delta t} = \frac{\frac{v_{C_1}}{n}}{L_m} \tag{2.13}$$

The equivalent circuit is shown in Fig. 2.8(B)

MODE 3 [t_2-t_3]:

At instant t_2 the switch is opened, causing diodes D_1 to conduct. During this interval, diode D_3 is still conducting. The equivalent circuit is shown in Fig. 2.8(C). This interval ends when the input current equals the magnetizing current and therefore the clamping diode current goes to zero. At the end of the interval the flyback diode starts to conduct. The leakage inductance current slope is determined by eq. 2.14

$$\frac{\Delta i_{lk}}{\Delta t} = -\frac{v_{C_1} + \frac{v_{C_1}}{n} - V_{in}}{L_{lk}} \tag{2.14}$$

The magnetizing current slope is determined by eq. 2.15

$$\frac{\Delta i_m}{\Delta t} = \frac{\frac{v_{C_1}}{n}}{L_{lk}} \tag{2.15}$$

MODE 4 [t_3-t_4]:

Once diode D_3 is turned off, the magnetizing current starts to decrease, transfering energy to the secondary side. The leakage inductance delivers its energy into capacitor C_1. The equivalent circuit is shown in Fig. 2.8(D)

The leakage inductance current slope is determided by eq. 2.16.

$$\frac{\Delta i_{lk}}{\Delta t} = -\frac{v_{C_1} - V_{in} - \frac{v_{C_2}}{n}}{L_{lk}} \tag{2.16}$$

The magnetizing inductance current slope is determined by eq. 2.17.

$$\frac{\Delta i_m}{\Delta t} = -\frac{\frac{v_{C_2}}{n}}{L_m} \tag{2.17}$$

MODE 5 [t_4-t_5]:

At instant t_4 diode D_1 current goes to zero and only the flyback section continues to deliver energy through diode D_2. The magnetizing current slope is determined by eq. 2.17.

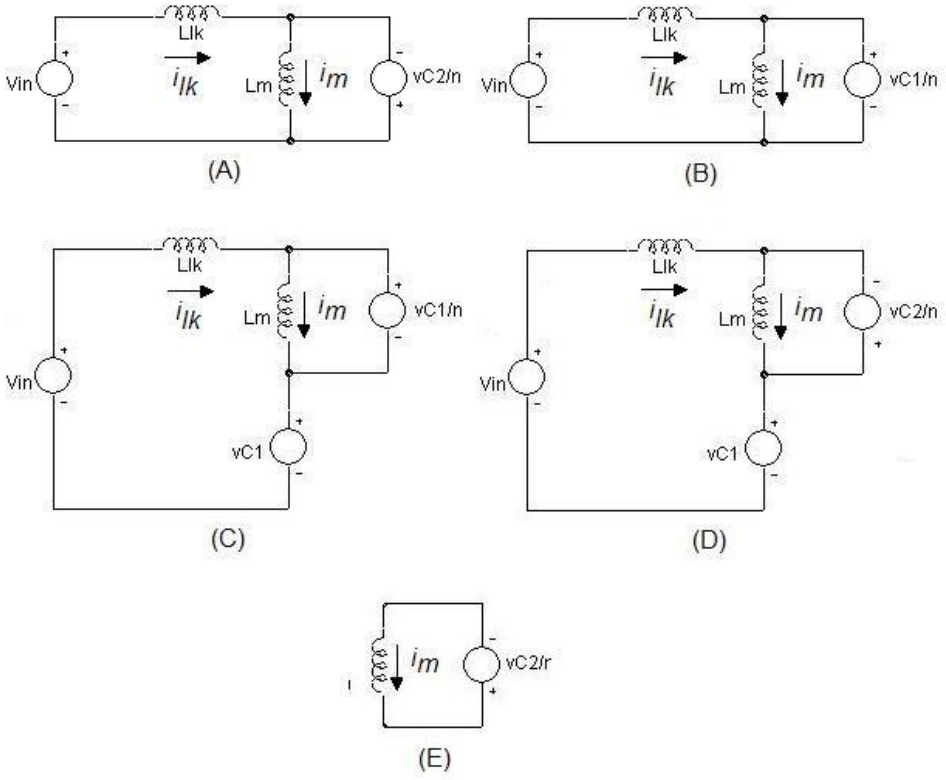

Figure 2.8: Sub-circuits in a switching period. (A) Mode1 (B) Mode2 (C) Mode3 (D) Mode4 (E) Mode5.

Something important to note at this point is the practical waveform obtained with the prototype, for the condition of input voltage equal to 25V, duty cycle equal to 0.68 and output current equal to 500mA. It shows a behaviour a little different from the one presented in the above discussion. See Fig. 4.1 and Fig. 4.2 of chapter 4 and the simulation results of Fig. 3.5 and Fig. 3.6 of chapter 3 for reference.

This difference can be explained by looking at the equation 2.12. The sign of the slope of the leakage inductance current is determined by the difference between the input voltage and the voltage of capacitor C_1, reflected on the primary side. This voltage depends on the duty cycle, load and other component parameters and values. Therefore it is reasonable to expect a change in sign on that slope depending on the circuit configuration.

Also important to realize is that before the clamping diode D_3 turns on, there is a resonance in the anode of the flyback diode caused by the parasitic inductances of transformer and parasitic capacitances of diodes. The high voltage at this point does not goes to zero instantaneously. Until it has reached zero, it causes a reflected voltage on the primary side of the transformer with a polarity inverted compared with the one shown in Fig. 2.8(B) and thus making the leakage inductance current to continue increase. Only after this voltage transition, the circuit is then governed by equation 2.12 and Fig. 2.8(B). This behaviour could be observed in the simulation when one of the circuit parameter, such as leakage inductance, was increased from 0.9uH to 1.1uH and this was in fact the behaviour observed in the prototype.

Chapter 3

Simulations

This chapter presents some simulations of the topologies explained in chapter 2. The simulations were carried out by means of SPICE based programs and the MATLAB toolbox PLECS which is a tool for simulation of electrical circuits within the Simulink environment. It is specially designed for power electronic systems and electrical drives. PLECS allows combined simulations of electrical circuits, thermal losses and controls.

3.1 Flyback-Boost Topology

Figure 3.1 shows the simulink model. It's an open loop power processing electrical model as defined by the box named *PLECS circuit* and shown in detail in Fig. 3.2. The output data of the simulation was also stored in the workspace MATLAB environment so further analysis or ploting could be done.

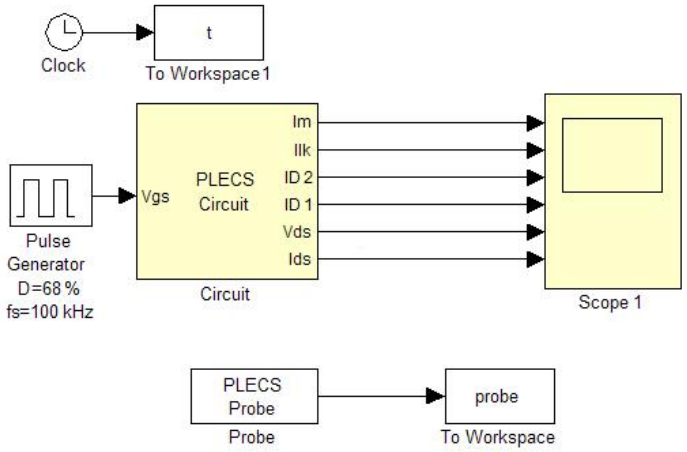

Figure 3.1: Simulink Model.

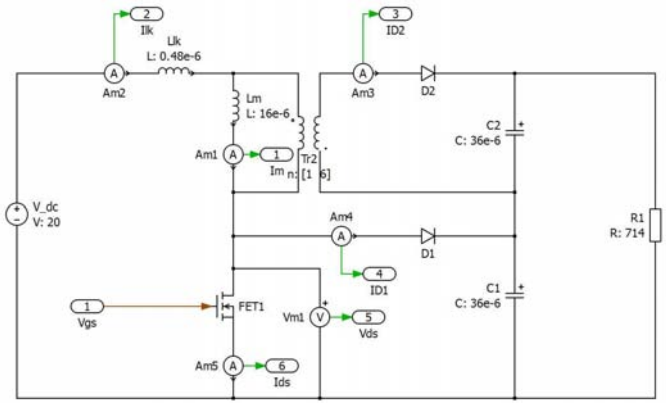

Figure 3.2: PLECS circuit.

Figure 3.3 shows the results for the currents as explained in section 2.2 of chapter 2.

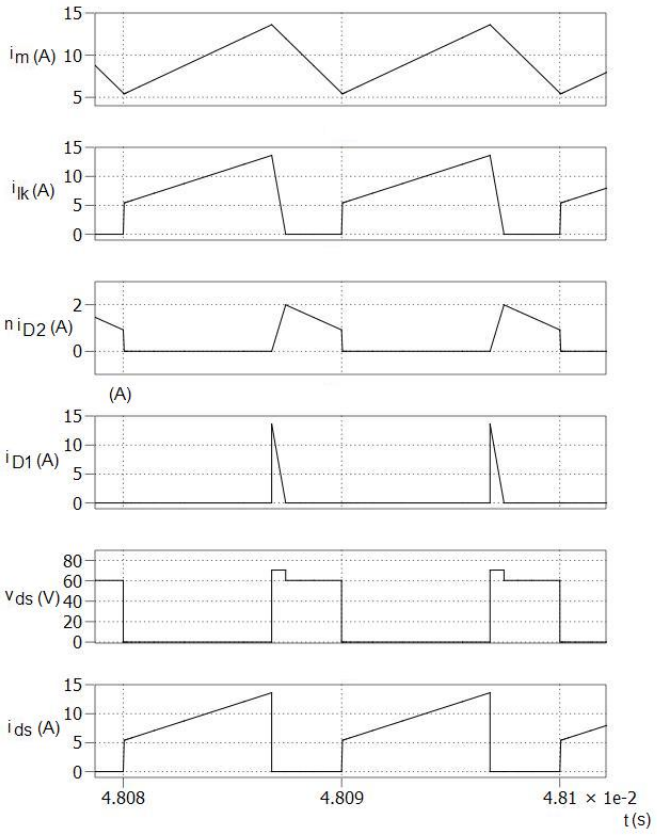

Figure 3.3: Simulated Waveforms.

3.2 Modified Flyback-Boost Topology

The waveforms presented in Fig. 3.5 and Fig. 3.6 are the results of SPICE based simulations of the circuit shown in Fig. 3.4. As already explained in section 2.4 the results presented in Fig. 3.5 agrees with the theoretical development presented in that section and Fig. 3.6 agrees with the practical waverforms obtained with the prototype and shown in section 4.

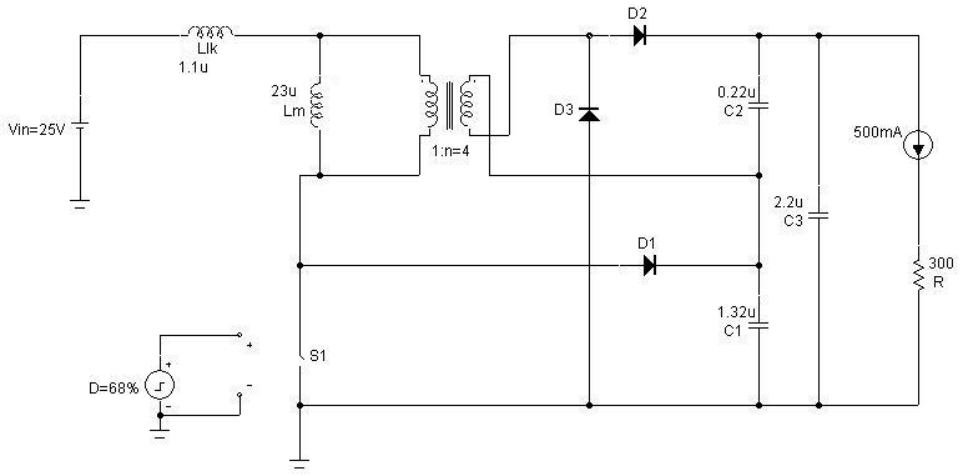

Figure 3.4: Simulated Circuit.

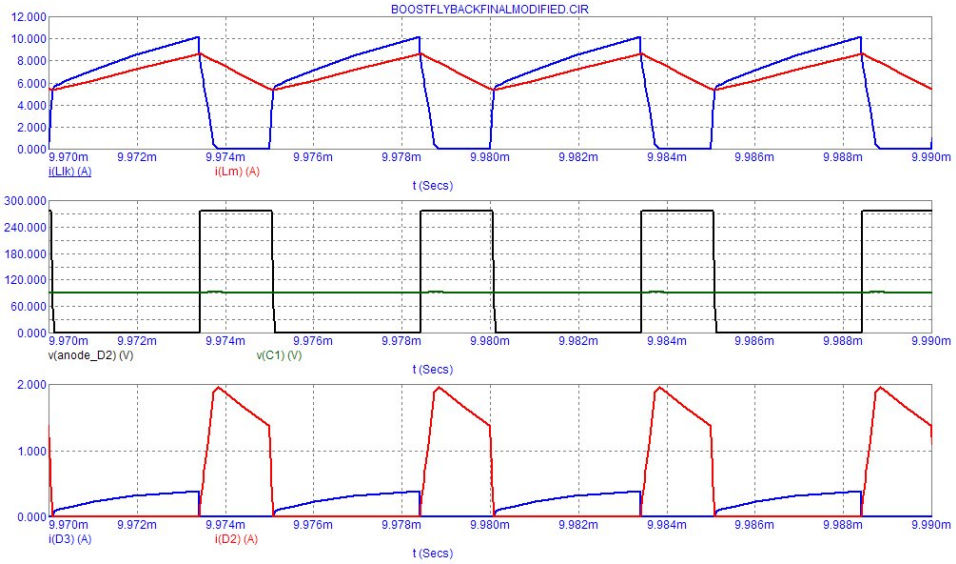

Figure 3.5: Simulation with Llk=0.9uH.

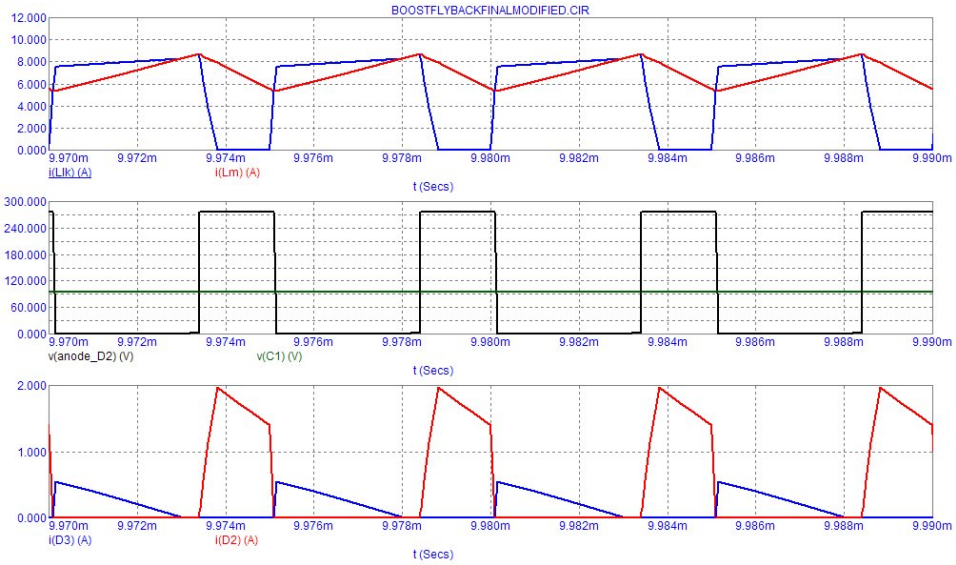

Figure 3.6: Simulation with Llk=1.1uH.

Chapter 4

Prototype Validation

The following results are regarded with the modified topology, that is, with the clamping diode introduced.

4.1 Waveforms

The waveforms of Fig. 4.1, Fig. 4.2 and Fig. 4.3 were obtained with the condition of input voltage equal to 25V, ouput voltage around 300V and output load equal to 500mA.

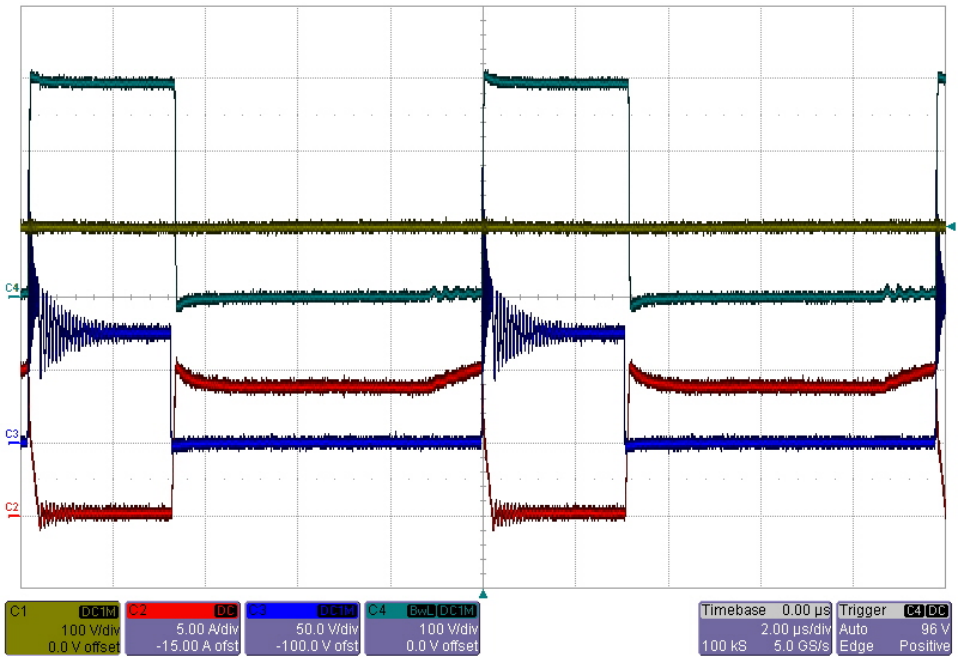

Figure 4.1: Waveforms. Ch1=V_{C1}, Ch2=i_{lk}=i_i, Ch3=v_{drain}, Ch4=$v_{anodoD2}$

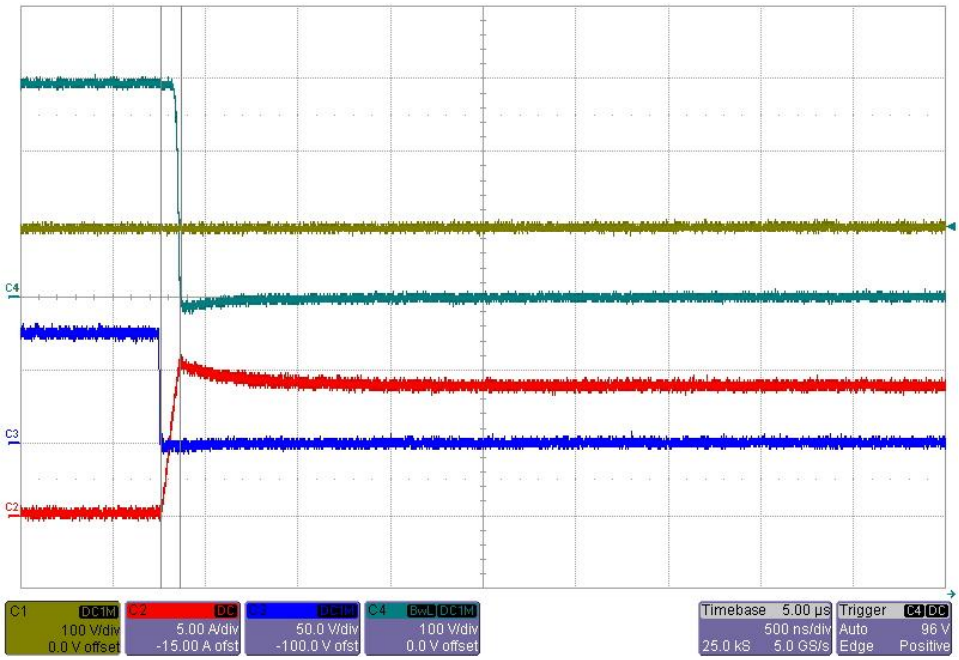

Figure 4.2: Zoom at Mosfet Turn-On. Ch1=V_{C1}, Ch2=i_{lk}=i_i, Ch3=v_{drain}, Ch4=$v_{anodoD2}$

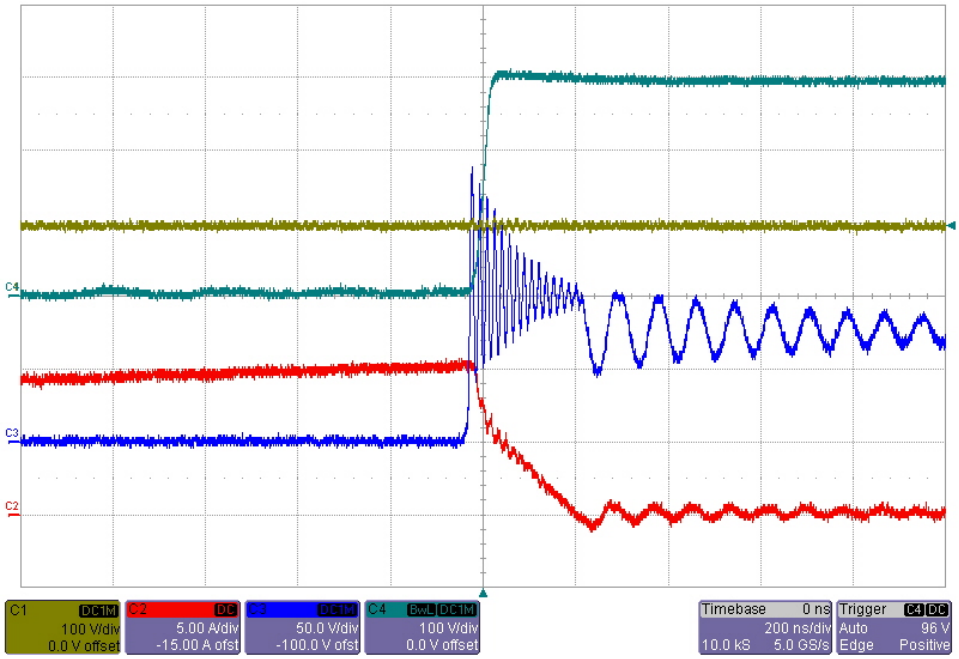

Figure 4.3: Zoom at Mosfet Turn-Off. Ch1=V_{C1}, Ch2=i_{lk}=i_i, Ch3=v_{drain}, Ch4=$v_{anodoD2}$

4.2 Efficiency Measurements

To see the effects of switching frequency, input voltage and load variations over the power losses, the prototype was submitted to different operating conditions and its efficiency was measured in all of them. The results are tabled in the next subsections.

4.2.1 Input Voltage Variation

Table 4.1: Measurements with V_o=400V I_o=0.5A F_s=200kHz

V_{in} (V)	I_{in} (A)	D (%)	η (%)
25	8.61	74.8	92.92
27	7.95	72,8	93.17
29	7.36	70.9	93.70
31	6.87	68.9	93.91
33	6.45	66.9	93.96
35	6.07	64.9	94.14

Table 4.2: Measurements with V_o=400V I_o=0.5A F_s=100kHz

V_{in} (V)	I_{in} (A)	D (%)	η (%)
25	8.44	75.2	94.79
27	7.81	73.4	94.85
29	7.25	71.5	95.12
31	6.77	69.5	95.30
33	6.37	67.6	95.14
35	6.00	65.6	95.24

Table 4.3: Measurements with V_o=400V I_o=0.75A F_s=200kHz

V_{in} (V)	I_{in} (A)	D (%)	η (%)
25	13.31	75.8	90.16
27	12.23	73,8	90.85
29	11.27	71.9	91.79
31	10.52	69.9	91.99
33	9.82	67.8	92.58
35	9.21	65.7	93.07

Table 4.4: Measurements with V_o=400V I_o=0.75A F_s=100kHz

V_{in} (V)	I_{in} (A)	D (%)	η (%)
25	12.85	75.8	93.39
27	11.86	74.00	93.69
29	11.02	72.1	93.87
31	10.24	70.1	94.51
33	9.60	68.1	94.70
35	9.04	66.1	94.82

4.2.2 Load Variation

Table 4.5: Measurements with V_{in}=25V V_o=400V F_s=100kHz

I_o (A)	I_{in} (A)	η (%)
0.75	12.92	92.88
0.625	10.67	93.72
0.500	8.50	94.12
0.375	6.34	94.64
0.250	4.22	94.79

Table 4.6: Measurements with V_{in}=35V V_o=400V F_s=100kHz

I_o (A)	I_{in} (A)	η (%)
0.75	9.05	94.71
0.625	7.51	95.11
0.500	6.00	95.24
0.375	4.50	95.24
0.250	3.03	94.30

The measurements results in section 4.2.1 where obtained with electrolytic input capacitor $C7$, as shown in the schematics appendix, while the measurements results in section 4.2.2 where obtained without this capacitor in the prototype. This fact, along with equipment tolerance, explain a small difference (about 60mA of input current) for input voltage of 25V and almost no difference for input voltage of 35V, when comparing equivalent operating conditions, presented in tables of these two sections.

4.3 Open Loop Transfer Function

It's not an easy task to derive a small a-c signal model for this topology using state-space averaging techniques. To get the duty-cycle to ouput voltage transfer functions, experimental data was used in place of mathematical models. Thus a network analyser was used to sweep the frequency of duty cycle perturbation over a certain operating condition. The results obtained can be viewed in Fig. 4.4 in four different dc operating points. One can see in Fig. 4.4(A), from the 1kHz to 10kHz decade, a decrease of 40dB in gain and a change of 180 degrees in phase, which indicates the presence of a pair of conjugate poles at the frequency around 1kHz.

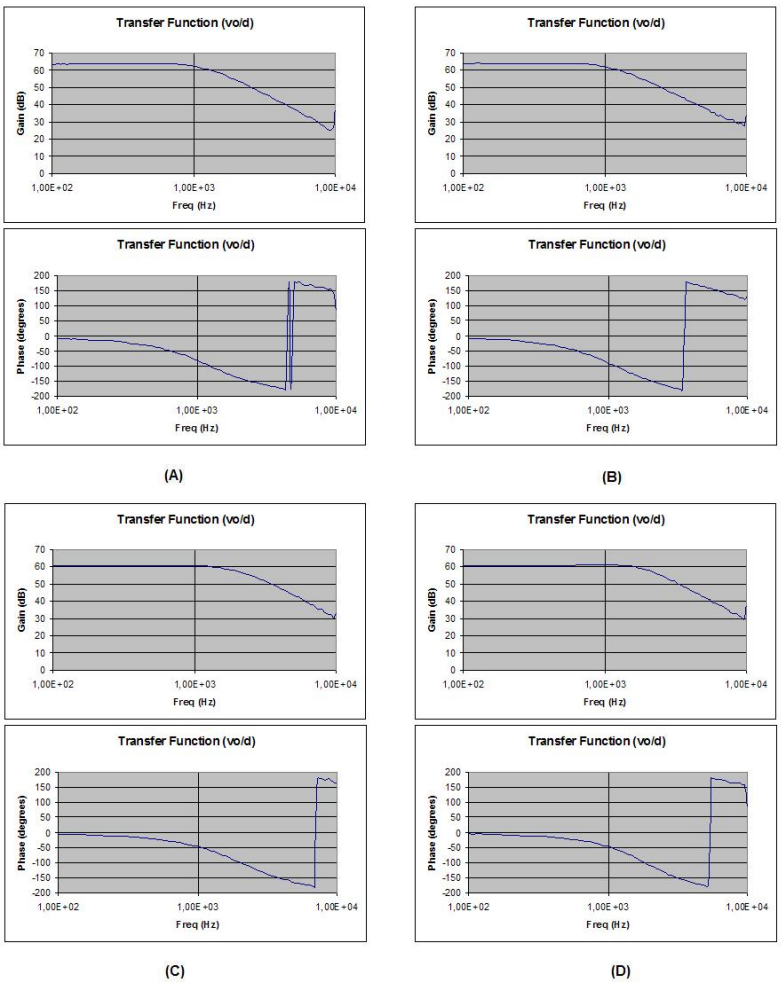

Figure 4.4: Duty-Cycle to Output Voltage Open Loop Transfer Functions. Output Voltage is 400V in all cases. (A)V_{in}=25V P_{out}=200W (B) V_{in}=25V P_{out}=300W (C) V_{in}=35V P_{out}=200W (D) V_{in}=35V. Pout=300W

Chapter 5

Conclusion

In this work the topology presented in [LTJ] was studied. The comprehensive and overall understading was improved, the main contributors of power losses were identified and then a modification was proposed [GSN] to improve efficiency. This modification was the introduction of a clamping diode as already discussed in previous chapters. With that, the need of a snubber across the flyback diode was not necessary anymore and energy was transferred directly from primary to secondary side.

Simulations were carried out with both the original and modified topologies. With the values obtained, it was realized that conduction losses on mosfet and diodes as well as the switching losses of mosfet sum up to a total that is aproximated equivalent to 4% of input power. This is in according to what is expected from this type of dc-dc converter that has high voltage ratio gain and consequently high rms currents at the primary side.

Also, a good amount of efficiency measurements were done in many different situations to verify the effect of load and input voltage variation and also the effect of switching frequency.

After that, the duty-cycle to output voltage gain and phase were measured experimentaly an the open loop transfer function was obtained. With the Bode plots in hand, it was designed a single integrator, with a very low bandwidth (around 20Hz and then around 10Hz). This dominant pole seemed to be sufficient to stably regulate the output voltage. But further analysis and new types of control could be tested in the prototype which can be suggested here as possible future works.

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Appendix A

Schematics

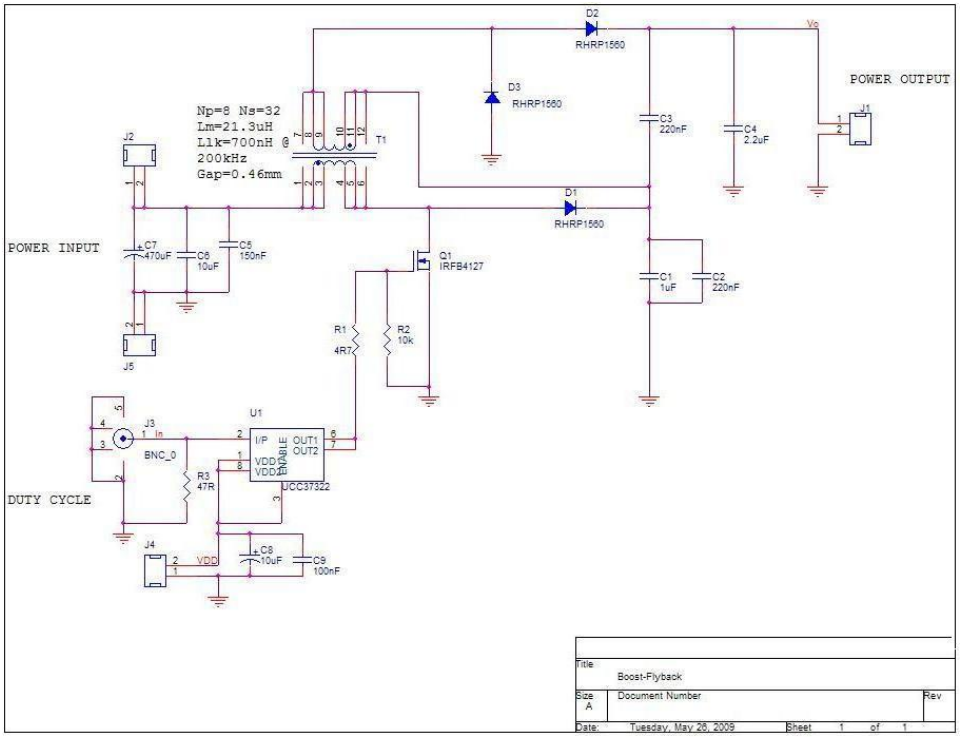

Figure A.1: Circuit Schematic

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